

Princess Sumaya University for Technology  
Computer Engineering Dept.  
22541 Computer Arch  
Fall 2023- First Exam



Princess Sumaya جامعة  
University الأميرة سميرة  
for Technology للتكنولوجيا

Name: *Solution* .....

Section: STT

Instructor: Amjed Al-Mousa

Duration: 55 minutes.

Date: 16/11/2023

Instructions:

- Exam consists of six questions, with a total of 25 points.
- Show your work; the final answer by itself does not count.
- Cellphones are not allowed.
- Calculators and RISC-V sheets are permitted.



Q1	/3	Q4	/6
Q2	/6	Q5	/4
Q3	/4	Q6	/2

Final Grade:

/25



**Question 1. Multiple Choice (3 points):**

Select the most appropriate answer

1. Suppose a computer needs to support 200 unique instructions. What is the minimum size of the opcode field? -assume there are no function fields like f3 and f7.
  - a) 200 bits
  - b) 7 bits
  - ☒ c) 8 bits
  - d) 9 bits
  - e) 64 bits
  
2. Two processors use the same architecture if the Execution time of Processor 1 is 3 times the execution time of Processor 2 for the same. Then which of the following is true:
  - a) P1 is faster than P2, with a ratio of 300%
  - ☒ b) P2 is faster than P1, with a ratio of 300%
  - c) P1 is faster than P2, with a ratio of 3%
  - d) P2 is faster than P1, with a ratio of 3%
  - e) We can't tell which is faster.
  
3. Static linking occurs at compilation time, whereas Dynamic linking occurs at runtime.
  - ☒ a) True
  - b) False



**Question 1. Multiple Choice (3 points):**

Select the most appropriate answer

1. Suppose a computer needs to support 300 unique instructions. What is the minimum size of the opcode field? -assume there are no function fields like f3 and f7.
  - a) 8 bits
  - ☒ b) 9 bits
  - c) 64 bits
  - d) 300 bits
  - e) 7 bits
2. Two processors use the same architecture if the Execution time of Processor 2 is 3 times the execution time of Processor 1 for the same task. Then which of the following is true:
  - a) P1 is faster than P2, with a ratio of 3%
  - b) P2 is faster than P1, with a ratio of 3%
  - ☒ c) P1 is faster than P2, with a ratio of 300%
  - d) P2 is faster than P1, with a ratio of 300%
  - e) We can't tell which is faster.
3. Static linking occurs at compilation time, whereas Dynamic linking occurs at runtime.
  - a) False
  - ☒ b) True

**Question 2. Computer Performance (6 points):**

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes (classes A, B, C, and D). The table below shows the clock rate for each processor and the CPI for each instruction class.

Processor	Clock Rate	CPI - A	CPI - B	CPI - C	CPI - D
P1	4 GHz	2	5	3	5
P2	3 GHz	3	3	3	3

- I. Given a program with a dynamic instruction count of  $2.0 \times 10^5$  instructions divided into classes as follows: 10% class A, 30% class B, 40% class C, and 20% class D,

- 1) What is the Average CPI for processors P1 & P2 for the given program? (2pt)

$$\text{a) } \text{CPI}_{P1} = 0.1 \times 2 + 0.3 \times 5 + 0.4 \times 3 + 0.2 \times 5 \\ = 0.2 + 1.5 + 1.2 + 1 = 3.9$$

$$\text{b) } \text{CPI}_{P2} = 3 \quad (\text{since all are 3})$$

- 2) What is the number of clock cycles required to execute the program on Processor 1? (1pt)

$$\# \text{ of cycles} = 3.9 \times 2 \times 10^5 = 7.8 \times 10^5$$

- 3) What is the CPU time to run the program on processor 2? (1pt)

$$\text{CPU time} = \frac{2 \times 10^5 \times 3}{3 \times 10^9} = 2 \times 10^{-4} = 0.2 \text{ ms}$$

- II. Suppose **a different program** needed 4 seconds to run on P1. Then we increased the frequency of P1 to 6 GHz, but this increase would result in a 20% increase in the number of instructions -these would be the same mix as the original instructions-. How much time would be needed to run the program with the new clock? (2pt)

$$\text{CPU time}_{\text{old}} = 4 \text{ sec.}$$

$$f_{\text{old}} = 4 \text{ GHz}$$

$$f_{\text{new}} = 6 \text{ GHz}$$

$$I_{\text{new}} = 1.2 \times I_{\text{old}}$$

$$\text{CPI}_{\text{new}} = \text{CPI}_{\text{old}}$$

$$4 = \frac{I_{\text{old}} \times \text{CPI}_{\text{old}}}{4 \times 10^9}$$

$$16 \times 10^9 = I_{\text{old}} \times \text{CPI}_{\text{old}}$$

$$\text{CPU time}_{\text{new}} = \frac{I_{\text{new}} \times \text{CPI}_{\text{new}}}{6 \times 10^9} = \frac{1.2 \times I_{\text{old}} \times \text{CPI}_{\text{old}}}{6 \times 10^9} \\ = \frac{1.2 \times 16 \times 10^9}{6 \times 10^9} = 3.2 \text{ sec.}$$

**Question 3: RISC-V Coding (4 points):**

Complete the missing values in the RISC-V code or the pseudo-code to match the functionality on the other side.

Assume f is stored in x10, g in x11, h in x12, i in x13, and j in x14. The base Address for Array A is at x15, and the base address for Array B is at x16. **Elements in A are word-sized, while elements in B are byte-sized.**

Pseudo-code	RISC-V Code
$A[3] = 8 * B[2]$	lb x2, 2(x16) slli x2, x2, 3 sw x2, 12(x15)
$A[6] = 8 * A[4*i] - 6$	slli x2, x13, 4 add x2, x2, x15 lw x3, 0(x2) slli x3, x3, 3 addi x3, x3, -6 sw x3, 24(x15)
if (i < j) f = g + h; else f = g - h;	bge x13, x14, Else add x10, x11, x12 jal x1, Exit Else: sub x10, x11, x12 Exit: ...

**Question 4. (6 points):**

In the code below, assume the PC is pointing at the instruction @ address 800. The initial register values are shown in the table to the right. Answer the following questions:

Memory		
Address	Instruction	
	800	Beq X0, X0, L2
	804	And X5, X5, X5
L1:	808	Sub X20, X7, X6
	812	Slli X10, X20, 2
	816	And X20, X21, X22
	820	Jal X1, Proc_A
	824	And X16, X20, X0
L2:	828	Add X6, X16, X7
	832	Beq X1, X2, L1
Exit:	836	
.....		
Proc_A:	944	Bltn X0, X10, Proc_A_Exit:
	948	Sub X10, X0, X10
Proc_A_Exit:	952	Jalr X0, 0 ( X1)
	956	0x408201b3

Register File	
Register	Value (Decimal)
X1	90
X5	100
X6	50
X7	400
X20	300

- What instruction will be executed after the one in address 800? (Write the full instruction)  
*Add X6, X16, X7*
- While Proc\_A is being executed, what is the value of X1?  
*824*
- Is the highlighted block of code considered a basic block of code?  
*No.*
- What is the immediate value stored in the instruction @address 800 (in place of L2)?  
 *$\frac{828 - 800}{2} = 14$*
- What is the value of X6, when the code reaches and executes the instruction @Address: 832?  
*400*
- What is the instruction stored at address 956?

0100 0000 1000 0010 0000 0001 1011 0011

*f<sub>7</sub>    rs<sub>2</sub>   rs<sub>1</sub>   f<sub>3</sub>   rd   op.*

*↓       ↓       ↓       ↓*

*x<sub>8</sub>   x<sub>4</sub>   x<sub>3</sub>   Sub*

*Sub X<sub>3</sub>, X<sub>4</sub>, X<sub>8</sub>*



**Question 5. (4 points):**

Assume the content of memory and registers as shown below, then find the value required after each of the following instructions:

(Note: Assume each branch starts fresh and does not depend on code in the previous branch)

Register	Content (Hex)
x1	0000 0000 0000 0005
x2	0000 0000 0000 0011
x3	0000 0000 0000 0040
x4	FFFF FFFF 0000 88BB
x5	FFFF FFFF 0000 2230
x6	FFFF FFFF 3232 3400
x7	0000 FFFF FFFF 0000
x8	0000 FFFF 0000 0005
x9	0000 FFFF 0000 0005
x10	FFFF 0000 0000 0100
x11	FFFF 0000 0000 0101
x12	FFFF 0000 0000 0102

Memory Address (Decimal)	Content (Hex)
1	00
2	45
3	F0
4	CB
5	E1
6	45
7	AC
8	2B
9	15
.....	.....
100	1F
101	3B
102	69
103	53
104	48
105	21
106	41
107	45
108	FF
109	AA

- Or x25, x5, x4  
x25 = ( 0x FFFF FFFF 0000 AABB )<sub>16</sub>
- lb x25, 2(x1)  
x25 = ( 0x FFFF FFFF FFFF FFAC )<sub>16</sub>
- lui x25, 1285 //FYI: (1285)<sub>10</sub> = (0x00505)<sub>16</sub>  
x25 = ( 0x 0000 0000 0050 5000 )<sub>16</sub>
- lb x25, 1(x1)  
sh x25, 1(x1)  
Mem [7] = ( 0x 0 0 )<sub>16</sub>

**Question 6. (2 points):**

A Computer program takes 120 seconds to execute on a single core. However, 60% of the program performance can be enhanced by using parallel programming on multiple cores. While the rest of the program can't be parallelized. What is the minimum speed-up factor needed so that the program would run in 72 seconds.

$$T_{\text{new}} = \frac{T_{\text{parallelizable}}}{n} + T_{\text{non-parallelizable}}$$

$$72 = \frac{0.6 \times 120}{n} + 0.4 \times 120$$

$$72 = \frac{72}{n} + 48$$

$$n = \frac{72}{72 - 48} = 3$$